Amendments to the Specification:

Please replace paragraphs 2, 3 and 4 on page 1 lines 5-20 with the following amended paragraphs:

U.S. Patent Serial No. 09/801,407 to Baskey et al. for INTER-PARTITION MESSAGE PASSING METHOD, SYSTEM AND PROGRAM PRODUCT FOR THROUGHPUT MEASUREMENT IN A PARTITIONED PROCESSING ENVIRONMENT ~~(Attorney Docket Number POU92000 0200US1)~~;

U.S. Patent Serial No. 09/801,993 to Kubala et al. for INTER-PARTITION MESSAGE PASSING METHOD, SYSTEM AND PROGRAM PRODUCT FOR MANAGING WORKLOAD IN A PARTITIONED PROCESSING ENVIRONMENT ~~(Attorney Docket Number POU92000 0201US1)~~; and

U.S. Patent Serial No. 09/802,185 to Baskey et al. for INTER-PARTITION MESSAGE PASSING METHOD, SYSTEM AND PROGRAM PRODUCT FOR A SHARED I/O DRIVER (~~Attorney Docket Number POU92000 0202US1)~~.

Please replace the first paragraph on page 17 lines 16 with the following amended paragraph:

Fig. 2 illustrates a high level representation of the elements constituting a physically partitioned processing system 200. As can be seen via reference to Fig. 2, the system 200 includes two domains or partitions A and B. Partition A is comprised of two system boards ~~201A1~~ 200A1 and ~~201A1~~ 200A2. Each system board of partition A includes memory 201A, processors 202A, I/O 203A and an interconnection medium 204A. Interconnection medium 204A allows the components on system board ~~201A1~~ 200A1 to communicate with one another. Similarly, partition B, which is comprised of a single system board 200B1 includes like constituent processing elements: memory 201B, processors 202B, I/O 203B and interconnect 204B. In addition to

the system boards grouped into partitions, there exists an interconnection fabric 205 which is coupled to each of the system boards and permits interconnections between system boards within a partition as well as the interconnection of system boards in different partitions.